Refine Search

Search Results -

Terms	Documents
monitor$3 near5 tim$3 near5 process$3 near5 activity	81

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L6	monitor$3 near5 tim$3 near5 process$3 near5 activity	81	L6
L5	monitor$3 near5 tim$3 near5 process$3 near5 (activity or operation)	390	L5
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DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2	23	L3
DB=USPT; PLUR=YES; OP=OR			
L2	monitor$3 near10 tim$3 near10 (processing near5 activity)	23	L2
L1	monitor$3 near10 tim$3 near10 (process$3 near5 activity)	111	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
monitor$3 near10 tim$3 near10 (processing near5 activity)	23

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L2	monitor$3 near10 tim$3 near10 (processing near5 activity)	23	L2
L1	monitor$3 near10 tim$3 near10 (process$3 near5 activity)	111	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L2	23

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

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DB=USPT; PLUR=YES; OP=OR			
L2	monitor$3 near10 tim$3 near10 (processing near5 activity)	23	L2
L1	monitor$3 near10 tim$3 near10 (process$3 near5 activity)	111	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

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DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
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L2	monitor$3 near10 tim$3 near10 (processing near5 activity)	23	L2
L1	monitor$3 near10 tim$3 near10 (process$3 near5 activity)	111	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(361/323 |361/683 |307/60 |340/636 |713/320 |713/321 |713/322 |713/323 |713/501 |713/600 |713/300).ccls.	5362

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L8

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

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L8	713/320-323,501,600,300;361/323,683;340/636;307/60.ccls.	5362	L8
L7	713/$3.ccls. and l6	17	L7
L6	monitor$3 near5 tim$3 near5 process$3 near5 activity	81	L6
L5	monitor$3 near5 tim$3 near5 process$3 near5 (activity or operation)	390	L5
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
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DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2	23	L3
DB=USPT; PLUR=YES; OP=OR			
L2	monitor$3 near10 tim$3 near10 (processing near5 activity)	23	L2
L1	monitor$3 near10 tim$3 near10 (process$3 near5 activity)	111	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L6 and L8	15

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L9

Refine Search

Recall Text | Clear | Interrupt

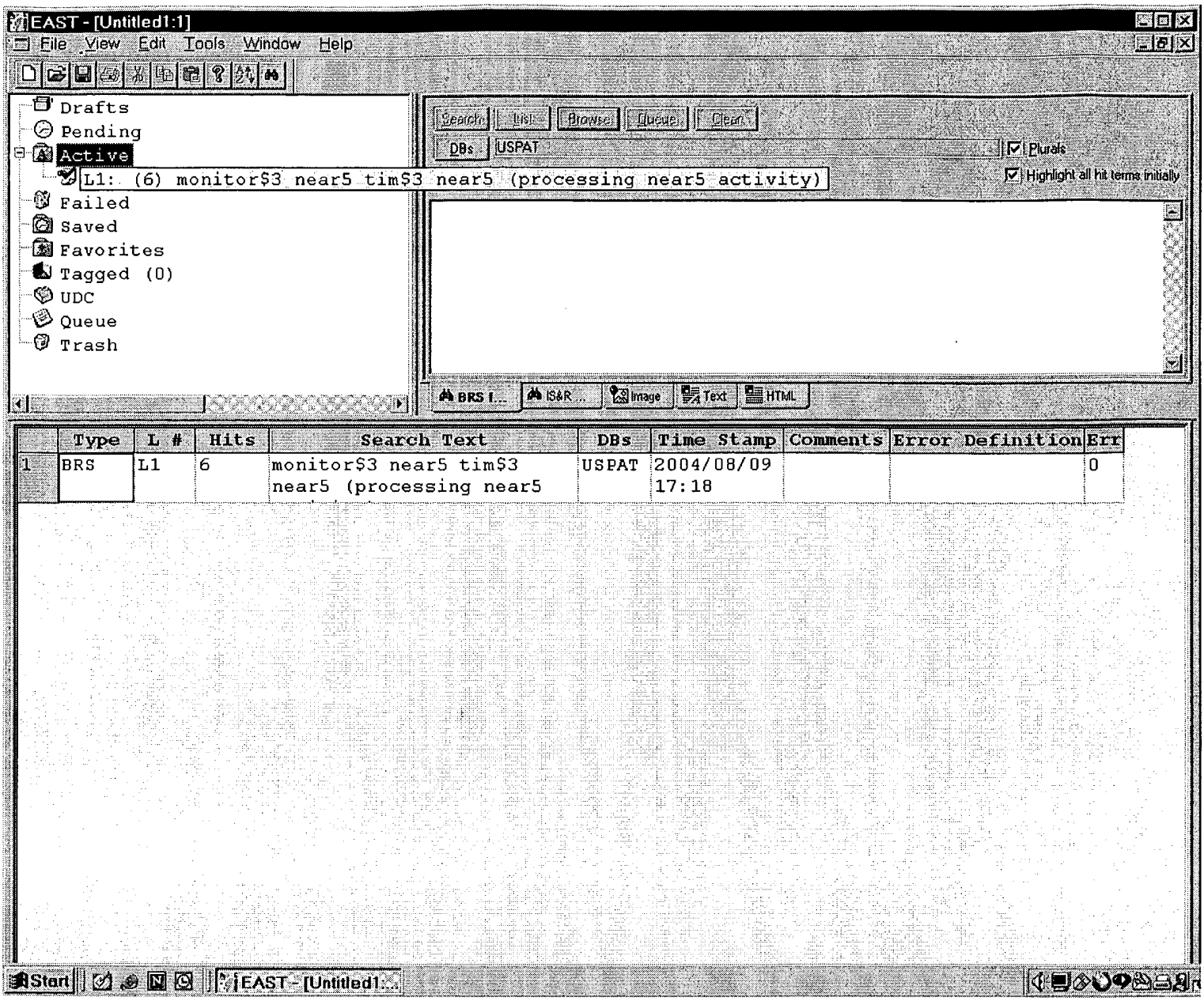
Search History

DATE: Monday, August 09, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L9	l6 and L8	15	L9
L8	713/320-323,501,600,300;361/323,683;340/636;307/60.ccls.	5362	L8
L7	713/$3.ccls. and l6	17	L7
L6	monitor$3 near5 tim$3 near5 process$3 near5 activity	81	L6
L5	monitor$3 near5 tim$3 near5 process$3 near5 (activity or operation)	390	L5
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	L2	23	L3
DB=USPT; PLUR=YES; OP=OR			
L2	monitor$3 near10 tim$3 near10 (processing near5 activity)	23	L2
L1	monitor$3 near10 tim$3 near10 (process$3 near5 activity)	111	L1

END OF SEARCH HISTORY

h e b b cg b e e ch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1 BRS L1 6 monitor$3 near5 tim$3 near5 (processing near5 USPAT 2004/08/09 17:18 0
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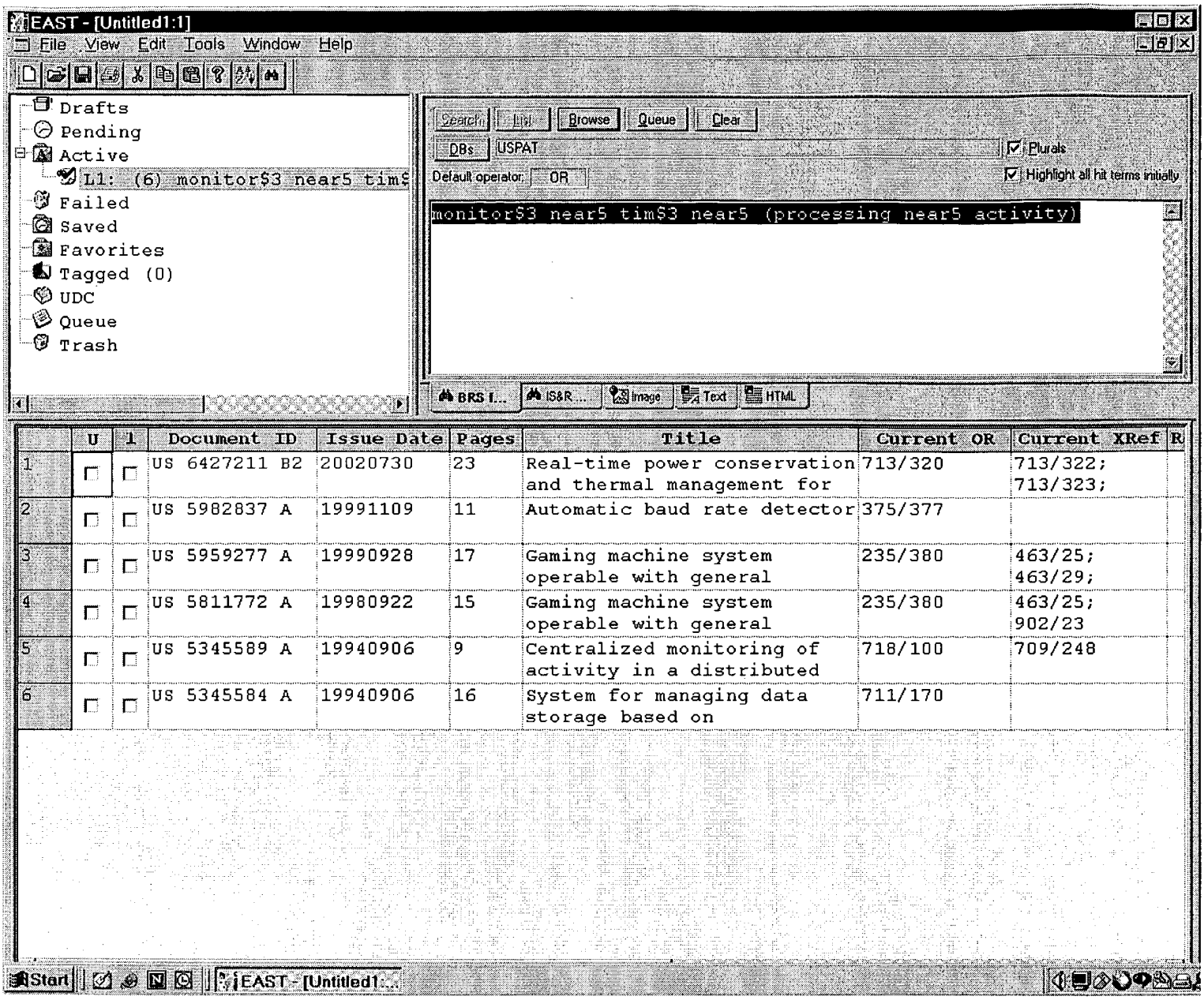
EAST - [Untitled1:1]
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Favorites
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Trash
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Plurals
Default operator: OR
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monitor$3 near5 tim$3 near5 (processing near5 activity)
BRS I... IS&R... Image Text HTML
U 1 Document ID Issue Date Pages Title Current OR Current XRef R
1 US 6427211 B2 20020730 23 Real-time power conservation and thermal management for 713/320 713/322; 713/323;
2 US 5982837 A 19991109 11 Automatic baud rate detector 375/377
3 US 5959277 A 19990928 17 Gaming machine system operable with general 235/380 463/25; 463/29;
4 US 5811772 A 19980922 15 Gaming machine system operable with general 235/380 463/25; 902/23
5 US 5345589 A 19940906 9 Centralized monitoring of activity in a distributed 718/100 709/248
6 US 5345584 A 19940906 16 System for managing data storage based on 711/170
Start
EAST - [Untitled1...

Your search matched **20** of **1060766** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

monitor* and tim* and process* and activity and (inc Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Monitoring neuronal oscillations and signal transmission between cortical regions using time-frequency analysis of electroencephalogra activity**
Haykin, S.; Racine, R.J.; Yan Xu; Chapman, C.A.;
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Pages:1295 - 1301

[Abstract] [PDF Full-Text (1012 KB)] **IEEE JNL**

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2 **Multi-channel EEG activity correlation analysis to detect the onset o cerebral ischemia**
Czinege, L.; Urbanics, R.; Farkas, Z.;
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Pages:1230 - 1231 vol.2

[Abstract] [PDF Full-Text (184 KB)] **IEEE CNF**

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3 **Circadian dynamics of respiratory parameters from ambulatory monitoring**
Raciti, M.; Pisani, P.; Emdin, M.; Carpeggiani, C.; Ruschi, S.; Kraft, G.; Francesconi, R.; Membretti, G.; Marchesi, C.;
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[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

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4 **Detection of seizures from small samples using nonlinear dynamic system theory**

Yaylali, I.; Kocak, H.; Jayakar, P.;
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5 **Practical solutions for the shutdown process in industrial facilities depending on network disturbances**
Drera, G.; Pedrazzini, S.; Previ, A.; Tonelli, L.;
Electricity Distribution, 2001. Part 1: Contributions. CIRED. 16th Internationa Conference and Exhibition on (IEE Conf. Publ No. 482) , Volume: 2 , 18-21 Ju 2001
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[Abstract] [PDF Full-Text (588 KB)] **IEE CNF**

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6 **Human EEG dimensionality and depth of anesthesia**
Watt, R.C.; Springfield, C.L.; Maslana, E.S.; Kanemoto, A.; Mylrea, K.;
Engineering in Medicine and Biology Society, 1994. Engineering Advances: Ne Opportunities for Biomedical Engineers. Proceedings of the 16th Annual International Conference of the IEEE , 3-6 Nov. 1994
Pages:223 - 224 vol.1

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7 **Bird hazard detection with airport surveillance radar**
Bruder, J.A.; Cavo, V.N.; Wicks, M.C.;
Radar 97 (Conf. Publ. No. 449) , 14-16 Oct. 1997
Pages:160 - 163

[Abstract] [PDF Full-Text (324 KB)] **IEE CNF**

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8 **Electrochromic mechanism study of corona poled electro-optic poly films**
Chen Gangjin; Xia Zhongfu; Zhang Yewen;
Properties and Applications of Dielectric Materials, 2000. Proceedings of the 6 International Conference on , Volume: 2 , 21-26 June 2000
Pages:741 - 744 vol.2

[Abstract] [PDF Full-Text (268 KB)] **IEEE CNF**

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9 **On-line testing for VLSI**
Nicolaidis, M.;
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10 **Time-frequency signal analysis applied to EEG signals associated w eye blinks**
Varner, J.L.; Rohrbaughz, J.W.; Sirevaag, E.J.; Packingham, K.; Stern, J.A.;
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Pages:1013 - 1014 vol.3

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11 **Content-based scalable H.263 video coding for road traffic monitor based on regularity of video content**
Ho, W.K.-H.; Lun, D.P.-K.;
Intelligent Multimedia, Video and Speech Processing, 2001. Proceedings of 2C International Symposium on , 2-4 May 2001
Pages:324 - 327

[Abstract] [PDF Full-Text (428 KB)] **IEEE CNF**

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12 **Taylor Enterprise Dynamics**
Nordgren, W.B.;
Simulation Conference, 2001. Proceedings of the Winter , Volume: 1 , 9-12 D 2001
Pages:269 - 271 vol.1

[Abstract] [PDF Full-Text (197 KB)] **IEEE CNF**

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13 **Heart rate variability after coronary artery bypass grafting**
Suda, Y.; Otsuka, K.; Ban, T.; Ichikawa, S.; Higashita, R.; Takeuchi, Y.;
Computers in Cardiology 1999 , 26-29 Sept. 1999
Pages:607 - 610

[Abstract] [PDF Full-Text (264 KB)] **IEEE CNF**

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14 **MIDAS-miniature intelligent domiciliary alarm system-a practical application of telecare**
Doughty, K.; Isak, R.; King, P.J.; Smith, P.; Williams, G.;
[Engineering in Medicine and Biology, 1999. 21st Annual Conf. and the 1999 Annual Fall Meeting of the Biomedical Engineering Soc.] BMES/EMBS Confere 1999. Proceedings of the First Joint , Volume: 2 , 13-16 Oct. 1999
Pages:691 vol.2

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15 **The TASTE-model and the EPM-system: conceptual designs for exploitation and exploration of aggregated emission inventory inform in environmental monitoring**
Misseyer, M.P.; Spoor, E.R.K.; Scholten, H.J.;
System Sciences, 1998., Proceedings of the Thirty-First Hawaii International Conference on , Volume: 7 , 6-9 Jan. 1998
Pages:428 - 440 vol.7

[Abstract] [PDF Full-Text (1164 KB)] **IEEE CNF**

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1 2 Next

Design verification of a super-scalar RISC processo

Turumella, B. Kabakibo, A. Bogadi, M. Menon, K. Thusoo, S. Nguyen, L. Saxena M.
HaL Comput. Syst., Campell, CA, USA ;

This paper appears in: **Fault-Tolerant Computing, 1995. FTCS-25. Digest Papers., Twenty-Fifth International Symposium on**

Meeting Date: 06/27/1995 - 06/30/1995
Publication Date: 27-30 June 1995
Location: Pasadena, CA USA
On page(s): 472 - 477
Reference Cited: 7
Inspec Accession Number: 5028582

Abstract:
The paper provides an overview of the design verification methodology for Ha **processor** development. This **activity** covered approximately two and a half design development **time**. Objectives and challenges are discussed and the v methodology is described. **Monitoring** mechanisms that give high observabili internal design states, novel features that **increase** the simulation speed, an automatic result checking are described. Also presented for the first **time**, is of the design defects discovered during the verification **process**. Such an ana useful in augmenting verification programs to target common design defects

Index Terms:
HaL Sparc64 **processor** development automatic result checking tools computer archi computer testing design defects design verification formal verification integrated cir internal design states **monitoring** mechanisms observability reduced instruction set simulation speed software tools super-scalar RISC **processor** verification programs machines HaL Sparc64 **processor** development automatic result checking tools con architecture computer testing design defects design verification formal verification circuit testing internal design states **monitoring** mechanisms observability reduced set computing simulation speed software tools super-scalar RISC **processor** verific programs virtual machines

Documents that cite this document
There are no citing documents available in IEEE Xplore at this time.

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US-PAT-NO: 6427211

DOCUMENT-IDENTIFIER: US 6427211 B2

TITLE: Real-time power conservation and thermal management for electronic devices

---------- KWIC ---------

Claims Text - CLTX (21):
21. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to optimize the utilization percentage of said processing unit.

Claims Text - CLTX (31):
31. An apparatus comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit in response to the utilization percentage of said processing unit being below a preselected level and/or temperature associated with said processing unit.

Claims Text - CLTX (33):
33. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit in response to one of: a) the utilization percentage of said processing unit being below a preselected level; b) temperature associated with said processing unit; and c) the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

(12) **United States Patent**
Watts, Jr.

(10) **Patent No.: US 6,427,211 B2**
(45) **Date of Patent: Jul. 30, 2002**

(54) **REAL-TIME POWER CONSERVATION AND THERMAL MANAGEMENT FOR ELECTRONIC DEVICES**

(75) Inventor: **La Vaughn F. Watts, Jr.**, Austin, TX (US)

(73) Assignee: **Texas Instruments Incorporated**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/727,597**

(22) Filed: **Dec. 1, 2000**

Related U.S. Application Data

(62) Division of application No. 08/395,335, filed on Feb. 28, 1995, now Pat. No. 6,158,012, which is a continuation-in-part of application No. 08/023,831, filed on Apr. 12, 1993, now Pat. No. 6,005,336, which is a continuation of application No. 07/429,270, filed on Oct. 30, 1989, now Pat. No. 5,218,704.

(51) Int. Cl.[7] **G06F 1/32**; G05F 1/08

(52) U.S. Cl. **713/320**; 713/322; 713/323; 713/501

(58) Field of Search 713/501, 300, 713/321, 322, 323, 340, 320; 700/14; 714/14; 327/513; 702/130, 132

(56) **References Cited**

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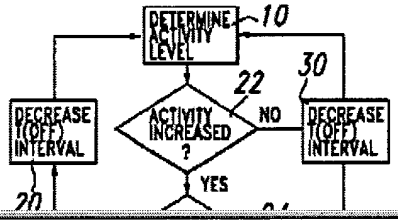
EP	0 501 655	A3	9/1992
EP	0 566 395	A1	10/1993
WO	WO 92/10032		6/1992

Primary Examiner—Gopal C. Ray
(74) *Attorney, Agent, or Firm*—Ronald O. Neerings; Wade James Brady, III; Frederick J. Telecky, Jr.

(57) **ABSTRACT**

A real-time power conservation and thermal management apparatus and method for portable computers employs a monitor (40) to determine whether a CPU may rest based upon a real-time sample of the CPU activity and temperature levels and to activate a hardware selector(500, 510, 520, 530) to carry out the monitor's determination. If the monitor determines the CPU may rest, the hardware selector reduces CPU clock time (280); if the CPU is to be active, the hardware selector returns the CPU to its previous high speed clock level (330). Switching back into full operation from its rest state occurs without a user having to request it and without any delay in the operation of the computer while waiting for the computer to return to a "ready" state. Furthermore, the monitor adjusts the performance level of the computer to manage power conservation and thermal management in response to the real-time sampling of CPU activity (10) and temperature (24). Such adjustments are accomplished within the CPU cycles and do not affect the user's perception of performance and do not affect any system application software executing on the computer.

65 Claims, 4 Drawing Sheets



L7: Entry 6 of 17 File: USPT Jan 9, 2001

DOCUMENT-IDENTIFIER: US 6173409 B1
TITLE: Real-time power conservation for electronic device having a processor

Current US Original Classification (1):
713/322

Current US Cross Reference Classification (1):
713/601

CLAIMS:

9. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU.

14. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU in response to usage of said CPU being below a preselected level.

15. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU to control the amount of activity time in said CPU.

16. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU to optimize the activity time within said CPU in response to usage of said CPU being below a preselected level.

17. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of idle time and activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU.

18. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of idle time and activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU in response to usage of said CPU being below a preselected level.

19. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of idle time and activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU to control the amount of idle time and activity time in said CPU.

24. An apparatus, comprising:

a central processing unit (CPU) having a monitor for measuring the relative amount of idle time and activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager selectively modifying a clock signal being sent to said CPU to control the amount of idle time and activity time in said CPU in response to a utilization percentage of said CPU being below a preselected level.

26. An apparatus, comprising:

a central processing unit (CPU) coupled to a clock and having a monitor for measuring the relative amount of idle time and activity time within said CPU; and

a clock manager coupled to said CPU, said clock manager controlling periods of time said clock is in an OFF state, the length of said periods of time said clock is in an OFF state being appropriate to allow said CPU to operate at an efficient utilization percentage.

Previous Doc Next Doc Go to Doc#

L7: Entry 6 of 17 File: USPT Jan 9, 2001

US-PAT-NO: 6173409
DOCUMENT-IDENTIFIER: US 6173409 B1

TITLE: Real-time power conservation for electronic device having a processor

DATE-ISSUED: January 9, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watts, Jr.; LaVaughn F.	Temple	TX		
Wallace; Steven J.	Temple	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 392205 [PALM]
DATE FILED: September 8, 1999

PARENT-CASE:
This application is a Continuation of application Ser. No. 08/023,831 filed Apr. 12, 1993 U.S. Pat. No. 6,006,336, which is a Continuation of application Ser. No. 07/429,270 filed Oct. 30, 1989, now U.S. Pat. No. 5,218,704.

INT-CL: [07] G06 F 1/32

US-CL-ISSUED: 713/322; 713/601
US-CL-CURRENT: 713/322; 713/601

FIELD-OF-SEARCH: 713/322, 713/601, 713/320, 713/300, 713/600

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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☐	3623017	November 1971	Lowell	
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☐	4819164	April 1989	Branson;
☐	4821229	April 1989	Jauregui
☐	4823292	April 1989	Hillion
☐	4823309	April 1989	Kusaka et al.
☐	4851987	July 1989	Day
☐	4870570	September 1989	Satoh et al.
☐	4893271	January 1990	Davis et al.
☐	4980836	December 1990	Carter et al.
☐	5025387	June 1991	Frane
☐	5083266	January 1992	Watanabe
☐	5086387	February 1992	Arroyo et al.
☐	5129091	July 1992	Yorimoto et al.
☐	5142684	August 1992	Perry et al.
☐	5167024	November 1992	Smith
	5179693	January 1993	Kitamura et al.

☐				
☐	5201059	April 1993	Nguyen	
☐	5218704	June 1993	Watts, Jr. et al.	
☐	5560024	September 1996	Harper et al.	
☐	5930516	July 1999	Watts, Jr. et al.	713/322

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 349 726 B1	January 1990	EP	
0 363 567 B1	April 1990	EP	
8911349	April 1990	EP	
0 349 726	October 1990	EP	

ART-UNIT: 271

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Neerings; Ronald O. Telecky, Jr.; Frederick J.

ABSTRACT:

A real-time power conservation apparatus and method for portable computers employs a monitor to determine whether a CPU may rest based upon a real-time sampling of the CPU activity level and to activate a hardware selector to carry out the monitor's determination. If the monitor determines the CPU may rest, the hardware selector reduces CPU clock time; if the CPU is to be active, the hardware selector returns the CPU to its previous high speed clock level. Switching back into full operation from its rest state occurs without a user having to request it and without any delay in the operation of the computer while waiting for the computer to return to a "ready" state. Furthermore, the monitor adjusts the performance level of the computer to manage power conservation in response to the real-time sampling of CPU activity. Such adjustments are accomplished within the CPU cycles and do not affect the user's perception of performance and do not affect any system application software executing on the computer.

31 Claims, 8 Drawing figures

Previous Doc Next Doc Go to Doc#

L7: Entry 5 of 17 File: USPT May 28, 2002

DOCUMENT-IDENTIFIER: US 6397340 B2
** See image for Certificate of Correction **
TITLE: Real-time power conservation for electronic device having a processor

Current US Original Classification (1):
713/322

Current US Cross Reference Classification (1):
713/601

CLAIMS:

11. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor.

18. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor in response to usage of said processor being below a preselected level.

19. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor to control the amount of activity time in said processor.

20. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor to optimize the activity time within said CPU in response to usage of said processor being below a preselected level.

21. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor.

24. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor in response to usage of said processor being below a preselected level.

25. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor to control the amount of idle time and activity time in said CPU.

30. An apparatus, comprising:

a processor having a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for selectively modifying a clock signal being sent to said processor to control the amount of idle time and activity time in said processor in response to a utilization percentage of said processor being below a preselected level.

32. An apparatus, comprising:

a processor coupled to a clock and having a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor for providing a signal for circuitry for controlling periods of time said clock is in an OFF state, the length of said periods of time said clock is in an OFF state being appropriate to allow said processor to operate at an efficient utilization percentage.

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L7: Entry 5 of 17 File: USPT May 28, 2002

US-PAT-NO: 6397340
DOCUMENT-IDENTIFIER: US 6397340 B2
**** See image for Certificate of Correction ****

TITLE: Real-time power conservation for electronic device having a processor

DATE-ISSUED: May 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watts, Jr.; LaVaughn F.	Austin	TX		
Wallace; Steven J.	Waco	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 756838 [PALM]
DATE FILED: January 9, 2001

PARENT-CASE:
This application is a Continuation of application Ser. No.09/392,205, filed Sep. 8, 1999,now U.S. Pat. No. 6,173,409 which is a Continuation of application Ser. No. 08/023,831, filed Apr. 12, 1993, now U.S. Pat. No. 6,006,336 which is a Continuation of application Ser. No. 07/429,270 filed Oct. 30, 1989, now U.S. Pat. No. 5,218,704.

INT-CL: [07] G06 F 1/32

US-CL-ISSUED: 713/322; 713/601
US-CL-CURRENT: 713/322; 713/601

FIELD-OF-SEARCH: 713/322, 713/323, 713/320, 713/300, 713/600, 713/601

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3453601	July 1969	Bogert et al.	
☐	3623017	November 1971	Lowell	
	3868647	February 1975	Zandvied	

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☐				
☐	3922526	November 1975	Cochran	235/152
☐	3941989	March 1976	McLaughlin et al.	
☐	4137563	January 1979	Tsunoda	
☐	4217637	August 1980	Faulkner et al.	
☐	4254475	March 1981	Cooney et al.	
☐	4267577	May 1981	Hashimoto et al.	
☐	4279020	July 1981	Christian et al.	
☐	4293927	October 1981	Hoshii	
☐	4316247	February 1982	Iwamoto	
☐	4317180	February 1982	Lies	
☐	4317181	February 1982	Teza et al.	
☐	4361873	November 1982	Harper et al.	
☐	4381552	April 1983	Nocilini et al.	
☐	4409665	October 1983	Tubbs et al.	
☐	4590553	May 1986	Noda	
☐	4612418	September 1986	Takeda et al.	179/81R
☐	4615006	September 1986	Maejima et al.	
☐	4670837	June 1987	Sheets	
☐	4686386	August 1987	Tadao	307/269
☐	4698748	October 1987	Juzswik et al.	
☐	4748559	May 1988	Smith et al.	
☐	4758945	July 1988	Remedi	
☐	4780843	October 1988	Tietjen	
☐	4814591	March 1989	Nara et al.	235/380
☐	4819164	April 1989	Branson	
☐	4821229	April 1989	Jauregui	
☐	4823292	April 1989	Hillion	
☐	4823309	April 1989	Kusaka et al.	
☐	4851987	July 1989	Day	
☐	4870570	September 1989	Satoh et al.	
☐	4893271	January 1990	Davis et al.	
☐	4980836	December 1990	Carter et al.	
☐	5025387	June 1991	Frane	
☐	5083266	January 1992	Watanabe	
☐	5086387	February 1992	Arroyo et al.	
☐	5129091	July 1992	Yorimoto et al.	
	5142684	August 1992	Perry et al.	

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☐				
☐	5167024	November 1992	Smith	
☐	5179693	January 1993	Kitamura et al.	
☐	5201059	April 1993	Nguyen	
☐	5218704	June 1993	Watts, Jr. et al.	
☐	5560024	September 1996	Harper et al.	
☐	6173409	January 2001	Watts, Jr. et al.	713/322

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 349 726	January 1990	EP	
0 363 567	April 1990	EP	
8911349	April 1990	EP	
0 349 726	October 1990	EP	

ART-UNIT: 2181

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Neerings; Ronald O. Brady, III; Wade James Telecky, Jr.; Frederick J.

ABSTRACT:

A real-time power conservation apparatus and method for portable computers employs a monitor to determine whether a CPU may rest based upon a real-time sampling of the CPU activity level and to activate a hardware selector to carry out the monitor's determination. If the monitor determines the CPU may rest, the hardware selector reduces CPU clock time; if the CPU is to be active, the hardware selector returns the CPU to its previous high speed clock level. Switching back into full operation from its rest state occurs without a user having to request it and without any delay in the operation of the computer while waiting for the computer to return to a "ready" state. Furthermore, the monitor adjusts the performance level of the computer to manage power conservation in response to the real-time sampling of CPU activity. Such adjustments are accomplished within the CPU cycles and do not affect the user's perception of performance and do not affect any system application software executing on the computer.

38 Claims, 8 Drawing figures

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L7: Entry 4 of 17 File: USPT Jul 30, 2002

DOCUMENT-IDENTIFIER: US 6427211 B2
TITLE: Real-time power conservation and thermal management for electronic devices

Current US Original Classification (1):
713/320

Current US Cross Reference Classification (1):
713/322

Current US Cross Reference Classification (2):
713/323

Current US Cross Reference Classification (3):
713/501

CLAIMS:

21. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to optimize the utilization percentage of said processing unit.

31. An apparatus comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit in response to the utilization percentage of said processing unit being below a preselected level and/or temperature associated with said processing unit.

33. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit in response to one of: a) the utilization percentage of said processing unit being below a preselected level; b) temperature associated with said processing unit; and c) the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

35. An apparatus comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to optimize the activity time in said processing unit.

37. An apparatus, comprising: a processing unit having a monitor for measuring the

relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to optimize the activity time within said processing unit in response to one of the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

39. An apparatus comprising: a processing unit having a monitor for measuring the relative amount of activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to optimize the activity time within said processing unit in response to one of: a) the utilization percentage of said processing unit being below a preselected level; b) temperature associated with said processing unit; and c) the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

41. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of idle time and activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to optimize the utilization percentage of said processing unit.

43. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of idle time and activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit in response to one of the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

45. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of idle time and activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit in response to one of: a) the utilization percentage of said processing unit being below a preselected level; b) temperature associated with said processing unit; and c) the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

47. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of idle time and activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to minimize the amount of idle time and optimize the activity time in said processing unit.

49. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of idle time and activity time within and temperature associated with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to minimize the amount of idle time and optimize the activity time in said processing unit in response to one of the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

51. An apparatus, comprising: a processing unit having a monitor for measuring the relative amount of idle time and activity time within and temperature associated

with said processing unit, results of said measuring being used by said processing unit for providing a signal for circuitry for selectively modifying a clock signal being sent to said processing unit to minimize the idle time and optimize the activity time within said processing unit in response to one of: a) the utilization percentage of said processing unit being below a preselected level; b) temperature associated with said processing unit; and c) the utilization percentage of said processing unit being below a preselected level and temperature associated with said processing unit.

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L7: Entry 4 of 17 File: USPT Jul 30, 2002

US-PAT-NO: 6427211
DOCUMENT-IDENTIFIER: US 6427211 B2

TITLE: Real-time power conservation and thermal management for electronic devices

DATE-ISSUED: July 30, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watts, Jr.; La Vaughn F.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 727597 [PALM]
DATE FILED: December 1, 2000

PARENT-CASE:
This application is a Divisional of application Ser. No. 08/395,335 filed Feb. 28, 1995 now U.S. Pat. No. 6,158,012, which is a Continuation-in-Part of application Ser. No. 08/023,831 filed Apr. 12, 1993 now U.S. Pat. No. 6,006,336, which is a Continuation of application Ser. No. 07/429,270 filed Oct. 30, 1989, now U.S. Pat. No. 5,218,704.

INT-CL: [07] G06 F 1/32, G06 F 1/08

US-CL-ISSUED: 713/320; 713/322, 713/323, 713/501
US-CL-CURRENT: 713/320; 713/322, 713/323, 713/501

FIELD-OF-SEARCH: 713/501, 713/300, 713/321, 713/322, 713/323, 713/340, 713/320, 700/14, 714/14, 327/513, 702/130, 702/132

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5167024	November 1992	Smith et al.	395/375
☐	5189314	February 1993	Georgiou et al.	307/271
☐	5287292	February 1994	Kenny et al.	364/550

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☐	5339445	August 1994	Gasztonyi	395/750
☐	5414860	May 1995	Canova, Jr. et al.	395/750
☐	5475847	December 1995	Ikeda	395/750
☐	5490059	February 1996	Mahalingaiah et al.	364/166
☐	5493684	February 1996	Gephardt et al.	395/750
☐	5502838	March 1996	Kikinis	395/550
☐	5504908	April 1996	Ikeda	395/750

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 426 410	May 1991	EP	
0 501 655	September 1992	EP	
0 566 395	October 1993	EP	
WO 92/10032	June 1992	WO	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Neerings; Ronald O. Brady, III; Wade James Telecky, Jr.; Frederick J.

ABSTRACT:

A real-time power conservation and thermal management apparatus and method for portable computers employs a monitor (40) to determine whether a CPU may rest based upon a real-time sample of the CPU activity and temperature levels and to activate a hardware selector(500, 510, 520, 530) to carry out the monitor's determination. If the monitor determines the CPU may rest, the hardware selector reduces CPU clock time (280); if the CPU is to be active, the hardware selector returns the CPU to its previous high speed clock level (330). Switching back into full operation from its rest state occurs without a user having to request it and without any delay in the operation of the computer while waiting for the computer to return to a "ready" state. Furthermore, the monitor adjusts the performance level of the computer to manage power conservation and thermal management in response to the real-time sampling of CPU activity (10) and temperature (24). Such adjustments are accomplished within the CPU cycles and do not affect the user's perception of performance and do not affect any system application software executing on the computer.

65 Claims, 8 Drawing figures

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L7: Entry 1 of 17 File: USPT May 4, 2004

DOCUMENT-IDENTIFIER: US 6732283 B2
TITLE: Processor having real-time power conservation

Abstract Text (1):
A processor, comprising a monitor for, depending on the respective embodiment, measuring the relative amount of idle time, activity time, or idle time and activity time within the processor, results of the measuring being used by the processor for controlling a clock speed of the processor. Yet other embodiments disclose, depending upon the respective embodiment, a processor, comprising a monitor for measuring the relative amount of idle time, activity time or idle time and activity time within the processor, results of the measuring being used by the processor to control power dissipation associated with the processor.

Current US Original Classification (1):
713/322

Current US Cross Reference Classification (1):
713/601

CLAIMS:

11. A processor, comprising: a monitor for measuring the relative amount of activity time within said processor, results of said measuring being used by said processor for controlling a clock speed of said processor.

21. A processor, comprising: a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor for controlling a clock speed of said processor.

32. A processor, comprising: a monitor for measuring the relative amount of activity time within said processor, results of said measuring being used by said processor to control power dissipation associated with said processor.

33. A processor, comprising: a monitor for measuring the relative amount of idle time and activity time within said processor, results of said measuring being used by said processor to control power dissipation associated with said processor.

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L7: Entry 1 of 17 File: USPT May 4, 2004

US-PAT-NO: 6732283
DOCUMENT-IDENTIFIER: US 6732283 B2

TITLE: Processor having real-time power conservation

DATE-ISSUED: May 4, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Watts, Jr.; LaVaughn F.	Austin	TX		
Wallace; Steven J.	Temple	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 10/ 375982 [PALM]
DATE FILED: February 28, 2003

PARENT-CASE:
This application is a Continuation of application Ser. No. 10/074,739, filed Feb. 11, 2002, which is a Continuation of application Ser. No. 09/756,838, filed Jan. 9, 2001, now U.S. Pat. No. 6,397,340 which is a Continuation of application Ser. No. 09/392,205, filed Sep. 8, 1999, now U.S. Pat. No. 6,173,409 which is a Continuation of application Ser. No. 08/023,831, filed Feb. 23, 1993, now U.S. Pat. No. 6,006,336 which is a Continuation of application Ser. No. 07/429,270 filed Oct. 30, 1989, now U.S. Pat. No. 5,218,704.

INT-CL: [07] G06 F 1/32

US-CL-ISSUED: 713/322; 713/601
US-CL-CURRENT: 713/322; 713/601

FIELD-OF-SEARCH: 713/300, 713/320, 713/322, 713/323, 713/324, 713/600, 713/601

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3453601	July 1969	Bogert et al.	
☐	3623017	November 1971	Lowell	

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☐	3868647	February 1975	Zandvied	
☐	3922526	November 1975	Cochran	
☐	3941989	March 1976	McLaughlin et al.	
☐	4137563	January 1979	Tsunoda	
☐	4217637	August 1980	Faulkner et al.	
☐	4254475	March 1981	Cooney et al.	
☐	4267577	May 1981	Hashimoto et al.	
☐	4279020	July 1981	Christian et al.	
☐	4293927	October 1981	Hoshil	
☐	4316247	February 1982	Iwamoto	
☐	4317180	February 1982	Lies	
☐	4317181	February 1982	Teza et al.	
☐	4361873	November 1982	Harper et al.	
☐	4381552	April 1983	Nocillini et al.	
☐	4409665	October 1983	Tubbs et al.	
☐	4590553	May 1986	Noda	
☐	4612418	September 1986	Takeda et al.	
☐	4615005	September 1986	Maejima et al.	
☐	4670837	June 1987	Sheets	
☐	4686386	August 1987	Tadao	
☐	4698748	October 1987	Juzswik et al.	
☐	4748559	May 1988	Smith et al.	
☐	4758945	July 1988	Remedi	
☐	4780843	October 1988	Tietjen	
☐	4814591	March 1989	Nara et al.	
☐	4819164	April 1989	Branson	
☐	4821229	April 1989	Jauregui	
☐	4823292	April 1989	Hillion	
☐	4823309	April 1989	Kusaka et al.	
☐	4841440	June 1989	Yonezu et al.	713/322
☐	4851987	July 1989	Day	
☐	4870570	September 1989	Satoh et al.	
☐	4893271	January 1990	Davis et al.	
☐	4924428	May 1990	Vea	714/1
☐	4980836	December 1990	Carter et al.	
☐	5025387	June 1991	Frane	
☐	5083266	January 1992	Watanabe	
	5086387	February 1992	Arroyo et al.	

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☐	5129091	July 1992	Yorimoto et al.
☐	5142684	August 1992	Perry et al.
☐	5167024	November 1992	Smith
☐	5175845	December 1992	Little
☐	5179693	January 1993	Kitamura et al.
☐	5201069	April 1993	Barabolak
☐	5218704	June 1993	Watts, Jr. et al.
☐	5222239	June 1993	Rosch
☐	5560024	September 1996	Harper et al.
☐	5930516	July 1999	Watts, Jr. et al.
☐	6006336	December 1999	Watts, Jr. et al.
☐	6173409	January 2001	Watts, Jr. et al.

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FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 363 567	September 1889	EP	
0 349 726	January 1990	EP	
0 349 726	January 1990	EP	
0 363 567	April 1990	EP	

OTHER PUBLICATIONS

"System Power Savings by Automatic Sleep Mode", IBM Technical Disclosure Bulletin, vol. 29, No. 9, Feb. 1987, pp. 4122-4124.
"Advanced Clock Controller Cuts Power Needs, Size of Static CMOS Systems", Curtis A. Mros and Walt Niewierski, Harris Corp., CMOS Technology, Design Entry, 6 pages.

ART-UNIT: 2181

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Neerings; Ronald O. Brady, III; Wade James Telecky, Jr.; Frederick J.

ABSTRACT:

A processor, comprising a monitor for, depending on the respective embodiment, measuring the relative amount of idle time, activity time, or idle time and activity time within the processor, results of the measuring being used by the processor for controlling a clock speed of the processor. Yet other embodiments disclose, depending upon the respective embodiment, a processor, comprising a monitor for measuring the relative amount of idle time, activity time or idle time and activity time within the processor, results of the measuring being used by the processor to control power dissipation associated with the processor.

33 Claims, 8 Drawing figures